A 2 Gb/s THROUGHPUT GaAs DIGITAL TIME SWITCH LSI USING LSCFL

Tohru Takada,* Yoshihiro Shimazu, Kimiyoshi Yamasaki,
Minoru Togashi, Keigo Hoshikawa, and Masao Idda

Atsugi Electrical Communication Lab., NTT,
3-1 Wakamiya Morinosato, Atsugi-shi, 243-01, Japan

*Musashino Electrical Communication Lab., NTT,
3-9-11 Midori-cho, Musashino-shi, Tokyo, 180, Japan

ABSTRACT

A GaAs four channel digital time switch having a 2.0 Gb/s throughput is developed. Low Power Source Coupled FET Logic (LSCFL) and 0.55 μm gate length buried p-layer SAINT-FETs are applied. The switch includes 1176 devices (FETs, diodes, and resistors). The 75 % fabrication yield is attained using dislocation free wafers.

INTRODUCTION

Recently, digital data processing in the Giga-bit rate range has become increasingly important for construction of the Information Network System (INS). Digital time switch LSIs are essential devices for exchanging data on a time multiplexed data highway. LSIs having throughput up to 192 Mb/s [1] have been obtained from Si LSI technology. Throughput is defined as channel number times channel data rate. Commercial digital time switch throughput is currently at a level of only 64 Mb/s for telephone data exchange.

A four channel digital time switch LSI having a 2.0 Gb/s throughput and a 500 Mb/s channel data rate was developed using GaAs MESFET technology. (In this circuit, maximum operation data rate is 2.0 Gb/s.) The channel data rate is sufficient for application to conventional 32 Mb/s TV data. Furthermore, it can be applied to 100 Mb/s or more High-Definition TV data transmission systems.

For present GaAs sequential logic technology [2], speed performance obtained during this experiment is the fastest to date (divider toggle frequency : typ. 5.1 GHz, max. 7.5 GHz). Also, dissipation power (1.4 mW/ equivalent gate) is the lowest, and integrated device number (1176 devices) is the largest yet obtained.

Three new aspects of GaAs LSI technology helped to achieve these performances and 75 % fabrication yield. First, a new circuit configuration was applied, named Low Power Source Coupled FET Logic (LSCFL). Second, a buried p-layer SAINT process [3] (BP-SAINT) was used, which fabricated 0.55 μm gate length FETs. Third, dislocation free semi-insulating wafers were processed. These wafers were grown by the FEC method [4].

This paper describes the circuit design, briefs the fabrication process, and examines the measurement results.

CIRCUIT CONFIGURATION

The digital time switch functions as a data exchange from input into output exchanged serial channel data as shown in Fig. 1. Address inputs control the output channel order. The LSI block diagram is shown in Fig. 2. The switch consists of 4-bit shift registers, data latches, a counter, a control unit and I/O buffer gates. Each circuit block is mainly constructed with R-S F/Fs, D-F/Fs, T-F/Fs, and 2-input OR/NOR gates. The total equivalent gate number is 231 gates. The maximum operational data rate is determined from the expression, $1/(6\,\tau_{pd})$. Here, τ_{pd} is the mean propagation delay time of internal series gates. Thus, the LSI operates at about 1/3 the toggle frequency of a frequency divider circuit operating at $1/(2\,\tau_{pd})$. Internal gate dissipation power is 1.4 mW per equivalent gate using a 20 μm FET gate width. Output, frame, and clock buffers dissipate 20, 30, 70 mW of power, respectively. Input buffers (data, clock, frame, and address) convert the ECL logic level into the LSCFL level defined as 0 ~ -0.45 V. The output buffer having a 100 ohm output impedance provides a 0.45 V LSCFL level.

The LSCFL circuit configuration was applied to the LSI. The LSCFL has true (D, C, Q) and

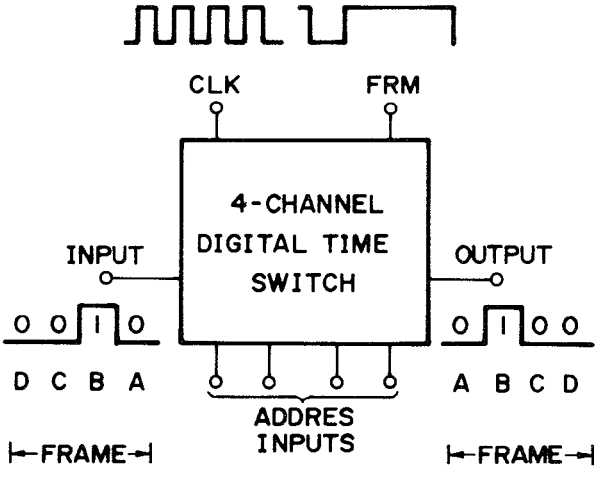

Figure 1 Function of Four-Channel Digital Time Switch.

complimentary ($\overline{D}$, $\overline{C}$, $\overline{Q}$) signal terminals at inputs and outputs as shown in Fig. 3(a). The R-S flip-flop using this configuration is shown in Fig. 3(b). The completely differential operation in LSCFL circuits enables the logic swing (V_{LS}) to be half of the V_{LS} for conventional SCFLs[5], where, $\overline{D}$ and $\overline{C}$ are used as reference DC voltage terminals. This is because the transfer gain using complimentary signals is 2 times larger than the SCFL operation using DC reference. The half V_{LS} represents half load resistance R_L, which implies higher speeds. It also requires a smaller voltage source magnitude V_{ss} implying lower power dissipation. The enhancement mode FET can also reduce the V_{ss} magnitude. V_{LS} and V_{ss} were determined to be 0.45 V and -2.5 V, respectively, using a +0.2 V FET threshold voltage V_{th}. The logic swing in LSCFL is small compared to other GaAs MESFET logics. However, the complimentary differential operation protects correct logic operation from fairly large device parameter deviations and scatterings. Simulation results show that LSCFL permits a deviation range of +0.2/-0.3 V for the 0.2 V centered V_{th}.

The experimental propagation delay of the LSCFL is 48 ps/gate (FI/FO=1/1) with 5.4 mW/gate. Dissipation power is effectively reduced to 1.4 mW/equivalent-gate by using series gate configurations. This power is much smaller than for other GaAs high speed logics, such as BFL (10 mW/gate), and is almost the same as DCFL. LSCFL drivability for interconnection line capacitance is also large due to the existence of source followers. Additional delay time per 1 mm line is measured to be 22 ps.

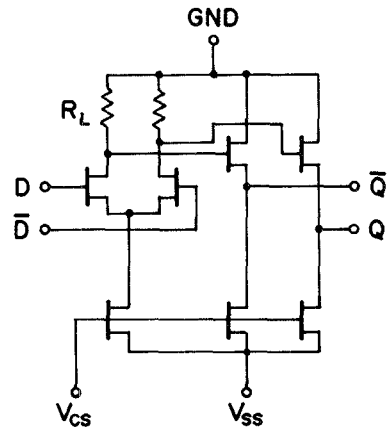

Figure 3(a) Inverter Configuration of LSCFL.

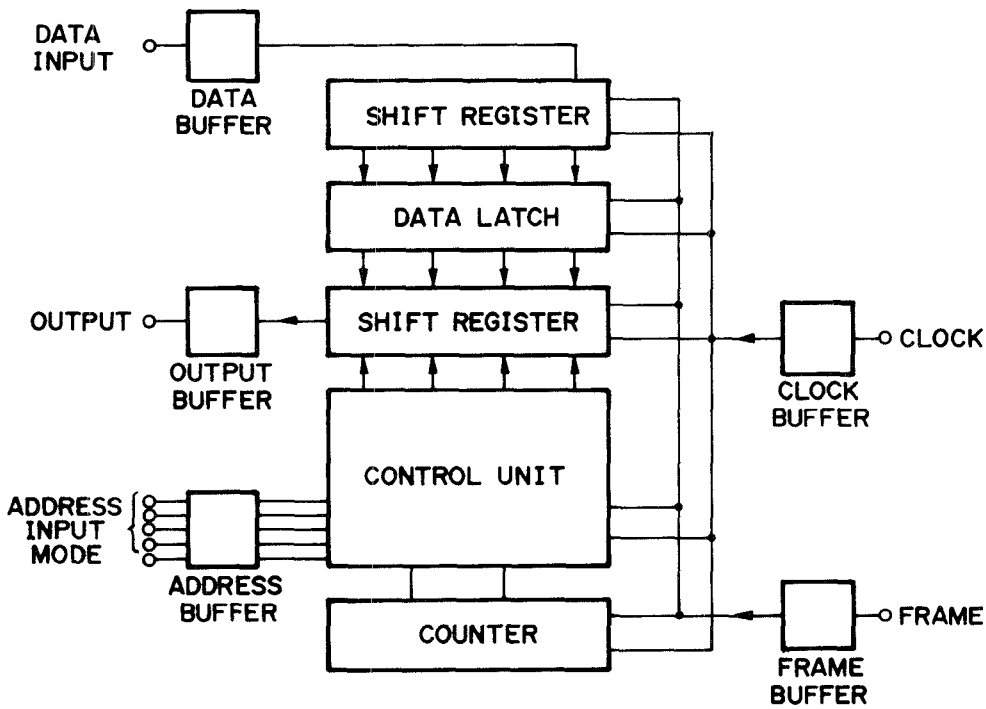

Figure 2 Block Diagram of Digital Time Switch.

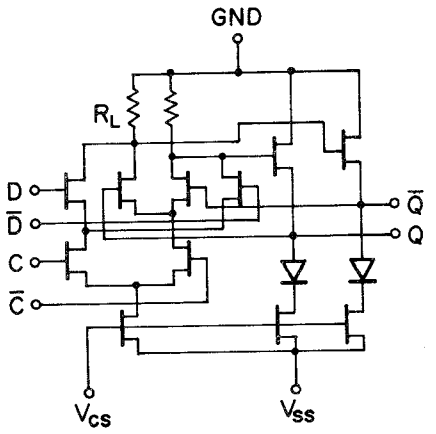

Figure 3(b) R-S Flip-Flop Configuration Using 2 Level Series Gate LSCFL.

FABRICATION PROCESS

Gate length shortening is the most effective method to obtain high performance FETs. However, FETs with submicron gate lengths present undesirable short channel effects, such as V_{th} reduction, large sub-threshold current, and V_{th} scattering increases. The buried p-layer SAINT process [3] was applied to decrease the short channel effects. As a result, 0.55 μm gate length FETs were successfully fabricated using photo-lithography with a 1/10 reduction stepper. In this process, a p-type layer is formed under the active layer to suppress substrate current by Be^+ implantation. The FET structure is shown in Fig.4.

Dislocations in LEC grown GaAs crystals induce V_{th} scattering.[6] Thus, dislocation-free wafers were used , which were obtained from the FEC method combined with induim doping.[4] A small measured V_{th} standard deviation of 49 mV in spite of submicron gate FETs is due to these wafers, as well as the buried p-layer FET process.

A brief description of the fabrication process and results are summarized in Table 1. A microphotograph of the LSI is shown in Fig. 5.

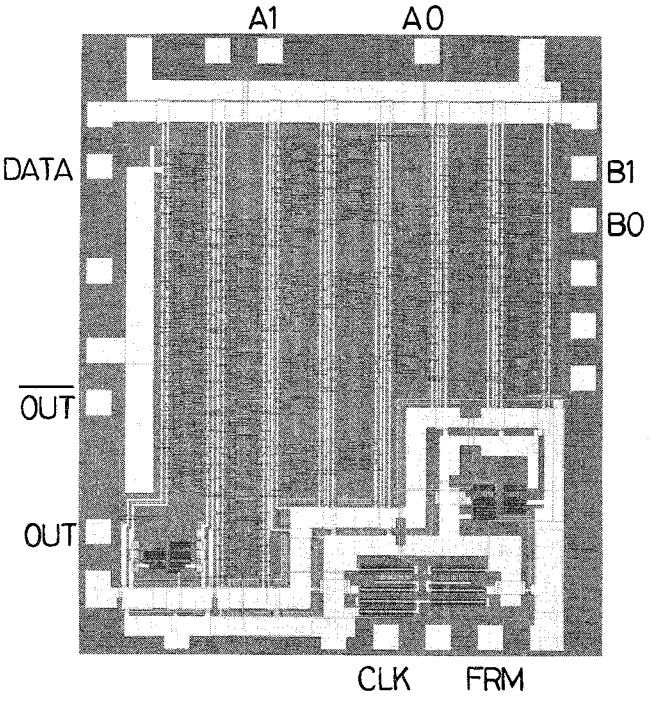

Figure 5 Microphotograph of Digital Time Switch. Chip size is 2.0×2.4 mm.

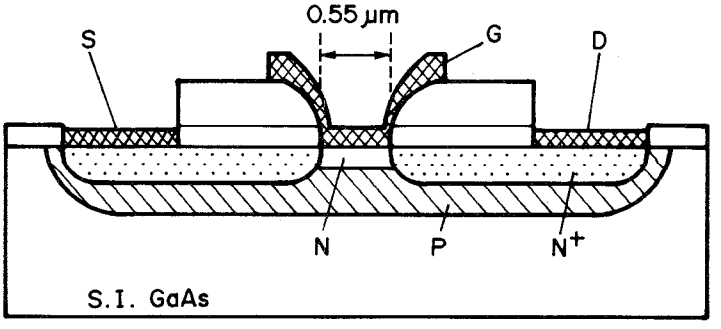

Figure 4 A Buried P-layer SAINT FET Structure.

TABLE 1 BP-SAINT FABRICATION PROCESS

Substrate	Dislocation-free LEC
	Photo-lithography 1:10 Stepper
Channel Layer	Si^+, 67 keV, 2.2×10^{12} cm^{-2} dose
N^+ Layer	Si^+, 200 keV, 4.0×10^{13} cm^{-2} dose
P layer	Be^+, 90 keV, 6.0×10^{11} cm^{-2} dose
Load Resistor	Si , 67 keV, 9.0×10^{12} cm^{-2} dose
Interconnection	1.5 μm line/space
Gate Length	0.55 μm
V_{th}	0.18 V
$\sim V_{th}$	49 mV
G_m	160 mS/mm
Load Resistor, R_L	880 ohm
$\sim R_L/R_L$	1.8 %

MEASUREMENT RESULTS

The measurement system was arranged with two 2.0 Gb/s word generators, a sampling oscilloscope, on-wafer probe card equipment, TTL-ECL transition ICs, and a personal computer. This arrangement is shown in Fig. 6. A PC9801 personal computer controlled the address input test pulse patterns. The 2 and 8 kinds of input and address data test patterns were used, respectively. Expected output patterns corresponding to input patterns, displayed on the computer CRT, were compared with measured output waveforms on the oscilloscope.

The fabricated LSI operated correctly for all test patterns up to and including the 2.0 Gb/s input data rate. Dissipation power is 0.64 W and V_{ss} is -2.5 V. A 2.0 Gb/s data exchange operation is shown in Fig. 7. It can be seen that the input

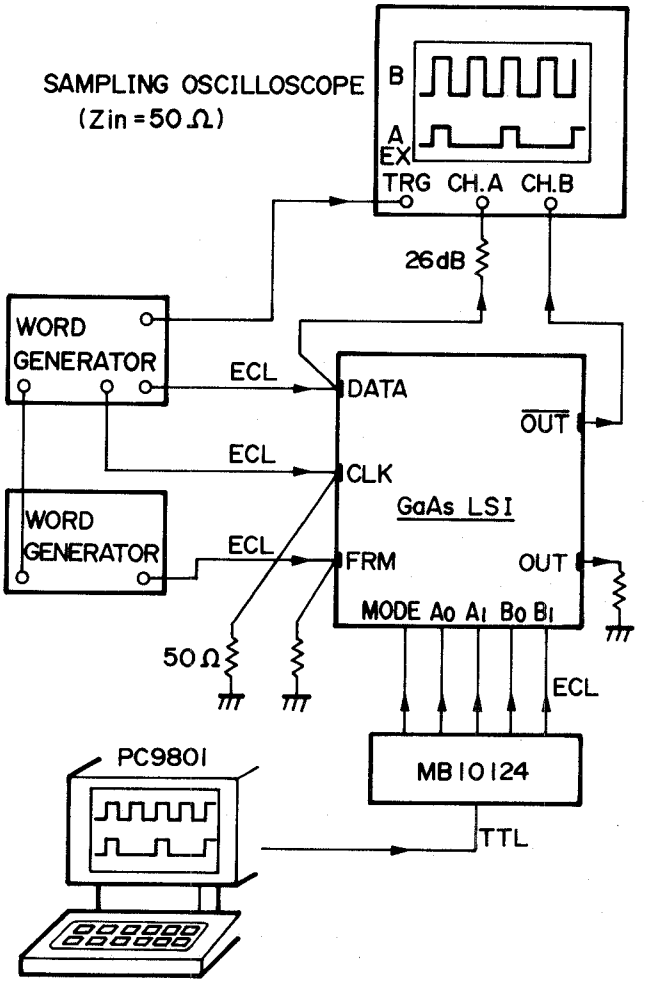

Figure 6 2.0 GHz Measurement System.

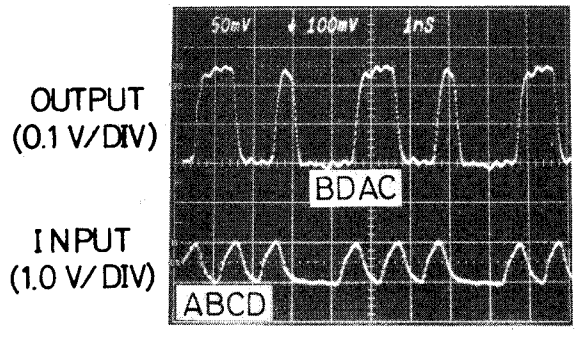

Figure 7 2.0 Gb/s Data Exchange Operation. Input channel data sequence, A, B, C, D is exchanged into output channel data sequence B, D, A, C.

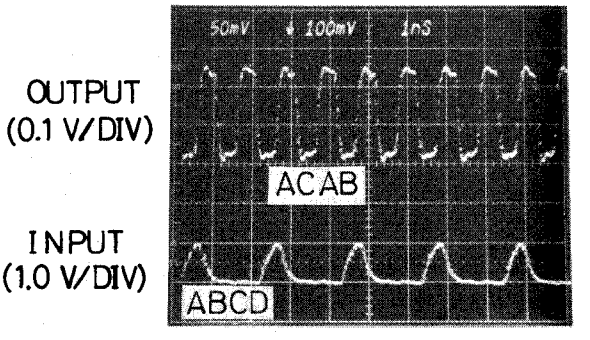

Figure 8 Plural Writing Exchange Operation. Input channel data, A, is written on two output channels.

channel order, ABCD, is exchanged into the output channel order, BDAC. The LSI also has a special function, which is that the same input data can be put on plural output channels. This is shown in Fig.8. Output wave rise and fall times (20 - 80 %) are 90 and 80 ps , respectively, as shown in Fig. 9. The range for correctly operating V_{ss} is from -1.7 to -3.0 V. The fabrication yield reached 63 % for the designed bias and 75 % for the adjusted bias. (V_{ss} is -2.5 V for both conditions)

To evaluate the internal gate operation speed, 1/4 frequency dividers were fabricated. These dividers had the same circuit configuration and device parameters, and was fabricated on the same wafer as the digital time switch. This divider operated up to 5.1 GHz with 45 mW of dissipation power. This result is reasonable, though this speed is not three times the maximum operation speed (2.0 Gb/s) of the digital time switch. This is because the digital time switch includes OR/NOR gates of FO=1 having smaller propagation delay times than for the divider (FO=3).

The divider toggle frequency increased to 7.5 GHz by increasing V_{ss} and V_{cs} (dissipation power was 277 mW) as shown in Fig.10. This value is currently highest of any frequency divider fabricated using GaAs MESFETs and HEMTs at room temperature.

CONCLUSION

A 2.0 Gb/s throughput GaAs digital time switch was developed using a new circuit configuration (Low Power Source Coupled FET Logic), a new fabrication process (buried P-layer SAINT), and dislocation-free wafers. In addition to high speed (48 ps/gate, 22 ps/mm) and low power (1.4 mW/equivarent-gate) performances, high fabrication yield of 75 % was achieved.

The LSI will have a favarable impact on constructing Giga-bit rate digital network systems.

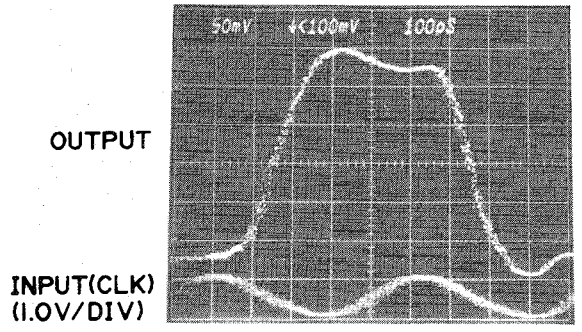

Figure 9 Output Wave Rise/Fall Time Measurement. Rise time is 90 ps, Fall time is 80 ps.

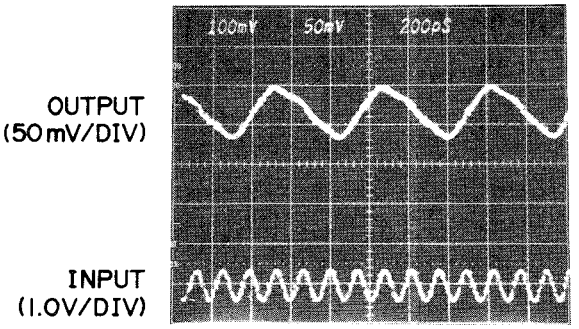

Figure 10 7.5 GHz Operation of 1/4 Divider

ACKNOWLEDGEMENT

The authors wish to acknowledge M. Hirayama, T. Sudo, and Y. Terada for helpful discussions and suggestions. They also wish to thank M. Ohmori, S. Miyazawa, N. Yasui, T. Sugeta, T. Ikegami and M. Fujimoto for their continuous encouragement.

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